Simulation Of Real Time 2D DWT Structure

الباحث

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ABSTRACT

The research was build fast structure that can decompose image by using DWT. The speed performance of the structure was tested using (Simulink) in (Matlab7).

This research is contain an introduction to the first works in this field, and describe the DWT which is the only kind that can be implement in the digital computer. The research was listing the important structures that are used to implement the digital filters which are the hart of DWT. The research is containing the problems that face us in my MSC thesis to implement DWT image structure processor. In MSC thesis we solve the problem of zero padding but we solve the second problem (waiting the column processor until the row processor finish its process) by using pipeline technique. The pipeline technique solves the problem partially. The research solve the second problem completely by proposing a new structure which make the 2D-DWT structure process the video in real time without waiting the row processor.

The results obtained from simulation of 2D DWT structure are compared with the MSC thesis results to show how we improve the process speed of 2D DWT structure.

1 Introduction

Vishiwanath is a researcher that suggest a structure that decompose a signal into multi-levels analyses (DWT levels), the proposed structure analyses the input signal and then re-input only the approximation signal to the same structure and so on in order to obtain the final level (the requested level) this structure is called the recursion structure. This structure take care the implementation cost but it cannot analysis the second signal until the process of the first one is complete (the delay time of the process of the first signal caused from the repetitive processing of the signal to receive the requested DWT level). For this reason the Seung-kwon propose the semi recursive structure. This structure is consist of two direct form structures, the first one analysis the signal one time and the other structure take care of the other analysis to receive the requested DWT level. This structure has little more than cost but it process the consecutive signals in real time (16).

Fan Wenbing, Gao Yingmin are suggest a 2D-DWT structure mainly consists of two one dimensional DWT units (1D-DWT) for horizontal and vertical transforms, a control unit realized as a finite state machine, and an internal memory block. For illustration see Fig 1. To process a sub-image, all rows are transferred to the FPGA over the PCI bus and transformed on the fly in the horizontal 1D-LWT unit using pipelining.

The coefficients computed in this way are stored in internal memory of different types. The coefficients corresponding to the rows of the sub image itself are stored in single port RAM. Now the vertical transform levels can take place. This is done by the vertical 1D-LWT unit. The control unit coordinates these steps in order to process a whole sub image and is responsible for generating enable signals, address lines, and so on(6).

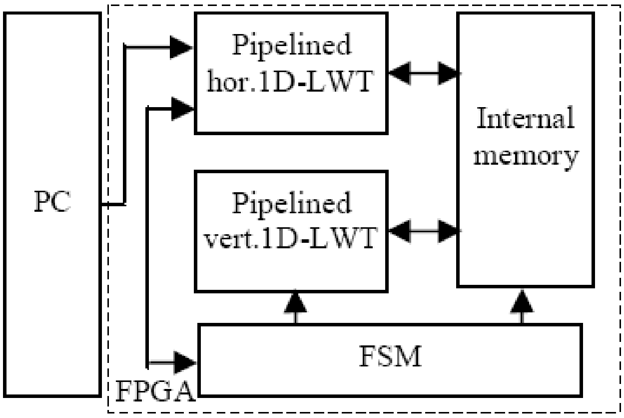


Figure (1) : block diagram of proposed structure

٢ Type of Wavelet Transform

There are three types of wavelet transforms according to the type of the basis used in the transform and the type of the processed signal (4)(11)

1. Continuous wavelet transform (CWT)
2. Semi-discrete wavelet transform (SDWT)
3. Discrete wavelet transform (DWT)

The important property in DWT transform is containing only multiplication and addition operations and this property is very suitable to digital computers (4). For this reason we concentrate in this type, and for more specific the fast one.

٢.2 Fast Wavelet Transform (FWT)

Mallat researches in 1989 prove that there is an opportunity to use digital filters instead of the two functions (Wavelet and Scaling functions) in DWT to increase the processing speed in this transform (14)(5). Mallat replace the Scaling function with low pass filter and the Wavelet function with the high pass filter (5).

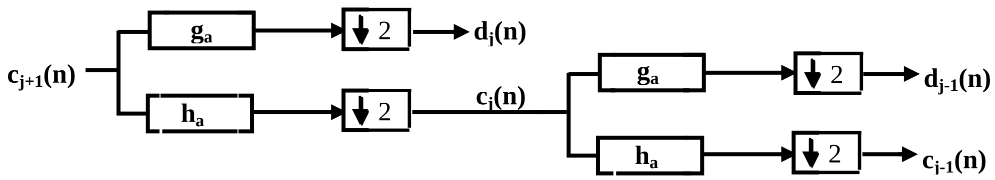
٢.2.1 Analysis Stage Of DWT

The following two equations are represent the analysis stage of FWT:

$$c_j(n) = \sum_{m=-\infty}^{\infty} h_a(m-2n)c_{j+1}(m) \qquad .....(1)$$

$$d_j(n) = \sum_{m=-\infty}^{\infty} g_a(m-2n)c_{j+1}(m) \qquad .....(2)$$

Where h_a is represent the low pass filter and g_a is representing the high pass filter. The following figure represents the analysis stage



Figure(2) two decomposition levels of DWT

We can compute the Detail or Scaling coefficients by the following equation:

$$M = floor(\frac{L+N-1}{2}) \qquad .....(3)$$

Where (floor) is represent the division quotient, L number of the samples in the discrete signal, N the length of the impulse response of the digital filter and M represent the number of the Scaling or Detail coefficients (9)(3).

٢.2.2 2D Discrete Wavelet Transform (2D-DWT)

This kind of transformation processes each row in the picture as one-dimensional signal. After the whole rows are processed in the picture, the same process is applied to the each column of the two pictures that resulted form the previous process. This process is illustrated in the following figure (8)(13)(1)(2)

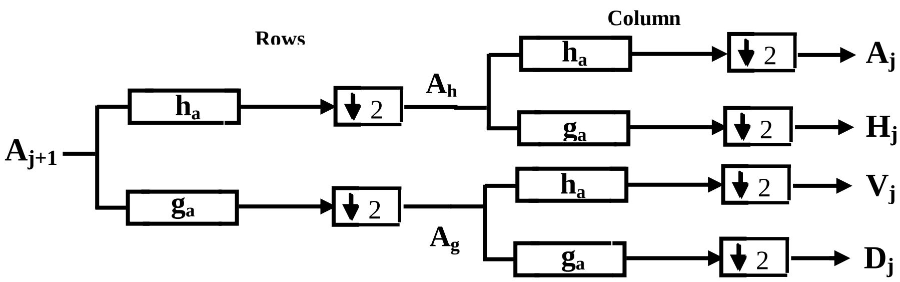


Figure (3) one stage of analysis 2D-DWT stage

٣ 1-D FIR Filter Structures

DWT use only FIR filters therefore we must know some structure to implement the hardware of these kinds of filters. Note in this paper the symbol N represents the number of the sample in the impulse response of the filter and h is the impulse response of the filter.

We can implement the FIR filter using one of the following structures:

٣.1 Direct Form Structure

An implementation can be directly derived from the definition of convolution in the time domain (12).

٣.2 Linear Phase Structure

A variation of the direct form structure is the linear phase structure, which takes advantage of the symmetry in the impulse response coefficients for linear phase FIR filters to reduce the computational complexity of the filter implementation.(7).

٣.3 Polyphase Filter Structure

If the filter coefficients are split into several individual filters through sampling of the impulse response, the derived filters are termed polyphase filters (12).

٣.4.1 Decimation Filters

The principle configuration for decimation is shown if figure below:

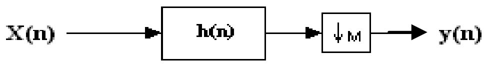


Figure (4) Decimation filter

An input sequence x is filtered, and every m-1 filtered value is used for the output sequence. The symbol (↓M) used is meant to represent sampling with a ratio of m:1 (12).

٣.4.2 Interpolation Filter

The structure of the interpolation filter is shown below: (15)

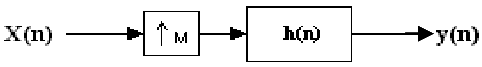


Figure (5) the interpolation filter

٤ 2D DWT structure

٤.1 The MSC 2D structure

The MSC thesis was use two processors (two 1D DWT structures) to construct the 2D DWT structure to process an image. The MSC thesis was introduce two different problems after simulation process, the first one was known the zero padding problem and The second problem is the 2nd processor cannot be operate until the 1st processor finish its job. The zero padding was needed to separate the successive rows or columns and the number of zero padded was equal to the impulse response of the filter minus one, this mean the processing time is grow up when the impulse response of the filter increased and vies versa. The two problems prevent the 2D DWT structure from decomposing a movie. The first problem was completely solved by using a proposed structure in my MSC thesis and the second problem was solved partially by using pipeline technique, this make MSC 2D DWT structure can decompose a movie. The pipeline technique is use the hardware professionally by making the 1st processor operate on the current image and the 2nd processor operate on the previous image, this means using pipeline technique hide the second problem not solve it (10).

٤.2 proposed 2D DWT structure

The 2D-DWT structure is consist of two 1D structures, the first one responsible for processing the row of the image and the second one is responsible for processing the column of the image. We use the same MSC proposed processor in the first processor. Our work is focused on the second processor (proposed structure) to make it process the partial results came from the first processor without waiting the whole column to be complete (whole image completion).

The image is growing up during convolution processing. The fig (6) is illustrate the image grow up caused by convolution process applied to each row and column of an image. The section A represent the original image and the sections B,C and D represents the samples added to the original image due to convolution process. The samples that added to image make it very difficult to process movie on the same processor using traditional structures so that the MSC 1D structure is split in to two parts, one for processing the row/column of the image and the second processing on the row/column tail.

The proposed structure is consist of two parts, the first part receive its input from the MSC row processor and work on each row sample one after another without waiting the completion of the row and have two outputs, the first output the part A of the current image and the second output the part C of previous image. The second part receives its input from MSC tail processor and work on each tail sample without waiting the completion of the tail and have two outputs, the first output part B of current image and the second output part D of the previous image. The four sections are operating on some times in parallel (when the image end and the structure receive new image). The figure (6) illustrates the part of the image.

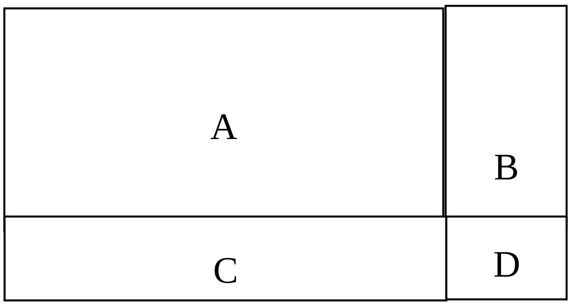


Figure (6) the convolution effects on image size

The proposed processor have the ability to process each sample without completion of the column because it make only the first step of the convolution and store the sample until the next sample come, on the other word the first step of the convolution applied onto the whole row, the second step of the convolution is applied onto the second row and the stored row (the first row) and so on. The number of the stored rows is equal to the number of the filter impulse response minus one and there is no need to store the whole image rows.

5 Results

We simulate the 2D DWT processor to process 256x256 images. The obtained results show the proposed structure decrease the response time of the 2D DWT processor to only the propagation delay time of two multipliers and two adders instead of the whole image receive time (65536 time unit) plus the propagation delay time of two multipliers and two adders. The compression between the two responses time we saw that the proposed 2D DWT processor save the image receive time and that mean it save a lot of time. The figure (7) illustrate the response time of the two 2D processors.

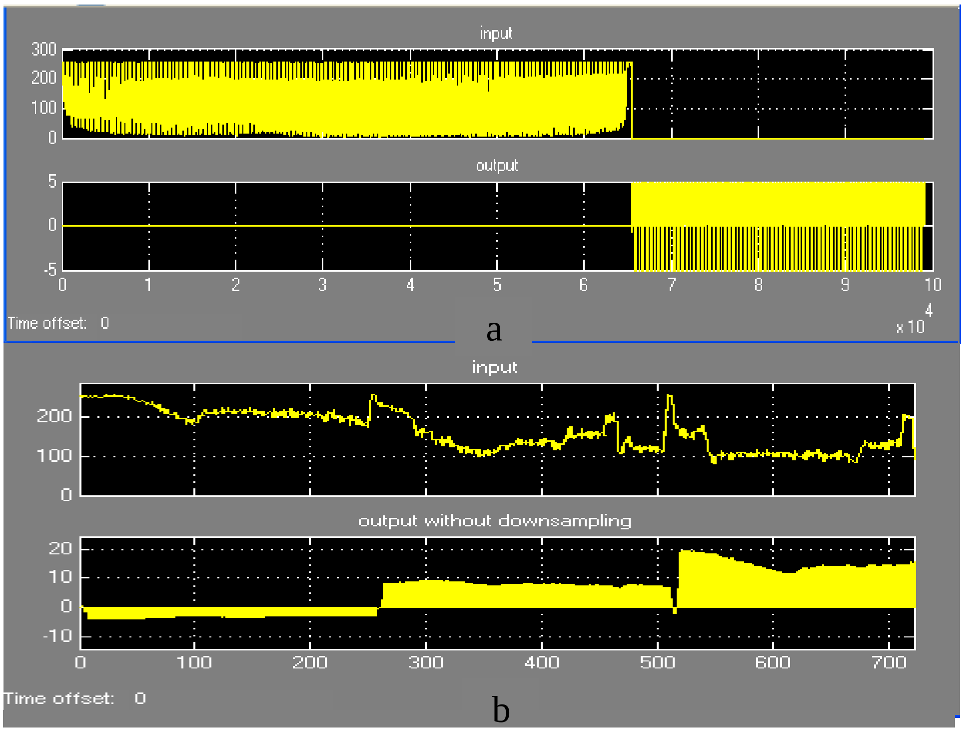


Figure (7) the response time of two processor: (a) the MSC processor (b) the proposed processor

The processing time of the image is also decreased, Figure (8) illustrate the processing time of three processors (proposed processor, the MSC processor and the traditional 2D processor) that process four images. The results in Figure (8) show that the processing time in proposed 2D DWT processor seem worse than MSC processor in the second image and so on images. The pipeline used in the MSC processor is making an illusion that the processing time decreased but in true the processing time still equal to the processing time of the first image. The MSC processor still consist from two stages one for rows and the other for columns, the columns stage still wait for completion of rows stage. The waiting problem is make the MSC processor output the decomposition of previous image while the proposed processor output the decomposition of the current image, this is make the proposed processor useful for processing real time movies.

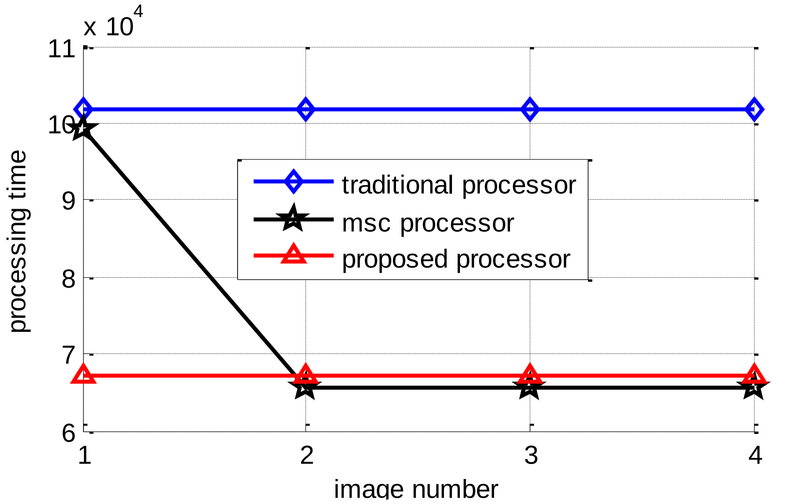


Figure (8) : the processing times of the three processors

The table (1) shows the processing times of the three processors and which of them can process movies. Table 1 show the processing time equal to the receive time (image size) plus 1534 time units. The additional delay time did not affect to the processing time of the next image because the proposed processor is use parallel processing technique. The proposed processor eliminate the storage unit to (N-1*row size) instead of the (2*decomposed row size*column size) in MSC processor.

Table 1 : The processing times of three processors in time unit

Processor	**First image processing time**	**Second image and so on images processing time**	**Movie processing**
Traditional processor	101781	101781	No
MSC processor	99086	65543	Yes
Proposed processor	67070	67070	Yes

6 Conclusions

The parallel processing was used in the proposed processor to make the processor process real time movies with the same clock used in the MSC processor and traditional processor. Using parallel processing is eliminates the storage number used and there is no need to use high speed components. The proposed processor was constructed from components that have propagation delay time approximately equal to sampling time this means the processor use cheapest component.

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محاكاة تنفيذ هيكل تحويل المويجة المقطع ذي البعدين خلال الزمن الحقيقي

الملخص

يتضمن هذا البحث امكانية بناء هيكل مادي سريع يقوم بتحليل المويجة المقطع للصور. سرعة اداء هذا الهيكل تم قياسها بعد محاكاته باستخدام برنامج (Simulink) الموجد في برنامج (Matlab7) .
يتكون هذا البحث من مقدمة حيث يستعرض فيها الاعمال السابقة ومن ثم استعراض لانواع تحويل المويجة وشرح مختصر عن تحويل الموجة المقطع والذي يعتبر النوع الوحيد القابل للتنفيذ رقمياً وكذلك يتم اسعراض لانواع الهياكل التي تستخدم لتنفيذ المرشحات الرقمية والتي تعتبر قلب تحويل المويجة المقطع.

يتضمن البحث استعراض المشاكل التي تواجهنا اثناء محاكات هياكل ذات البعدين لتحويل المويجة المقطع والتي اجريت في بحث الماجستير. تم اقتراح هيكل في بحث الماجستير لحل مشكلة اضافة الاصفار بصورة كلية ولكن المشكلة الثانية (مشكلة انتضار معالج الاعمدة الى ان ينتهي معالج الصفوف من معالجة الصورة) لم يتم حلها بصورة كلية حيث تم استخدام تقنية خط الانابيب لحل هذه المشكلة. البحث اقترح هيكل جديد لمعالجة المشكلة الثانية بصورة كلية وقد تم اسخدامه كجزء من اجزاء هيكل ذي البعدين وبذالك اصبح بامكانه معالجة الافلام بالزمن الحقيقي.

النتائج التي تم الحصول عليها اثناء محاكاة الهيكل المقترح تم مقارنتها مع النتائج التي تم الحصول نتيجة محاكاة عمل هيكل الماجستير والهيكل التقليدي لبيان مدى التحسن الحاصل في معالجة الافلام عند استخدام الهيكل المقترح.